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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/655,197	09/05/2000	Alfred I-Tsung Pan	10992304-1	7747

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EXAMINER

SOWARD, IDA M

ART UNIT PAPER NUMBER

2822

DATE MAILED: 12/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/655,197

Applicant(s)

PAN, ALFRED I-TSUNG

Examiner

Ida M Soward

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 September 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-13 and 22-25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-13 and 22-25 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

This Office Action is in response to Applicant's amendment filed September 8, 2003.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 4-9, 12-13, 22 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ho (4,254,445) in view of Yao (6,163,068), Ferri (4,326,180) and Houston (US 6,362,117 B1).

Ho teaches a common carrier, comprising: a carrier substrate **9** having an upper surface wherein the carrier substrate includes a plurality of slots **11** for adhering the plurality of chips, one chip per slot; a plurality of integrated chips **10** disposed on the upper surface and aligned with each other and the carrier substrate (Figure 1, col. 2, lines 57-68) and a glass substrate (cols. 1-2, lines 65-68 & 1-3, respectively). Ho further teaches the carrier substrate and the integrated chips each having parallel top surfaces which reside essentially within the same plane (Figure 1) and the carrier substrate and the integrated chips each having parallel top surfaces which do not reside within the same plane (Figure 3). However, Ho fails to teach lithographic alignment tolerances

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and adhesive bonds. Yao teaches integrated circuit chips **30** adhered to a carrier substrate **20** using an adhesive bond 50 (Figure 1, col. 2, lines 26-54). Ferri teaches at least two electrically conductive nodes **10, 22 & 26**, the electrically conductive nodes are disposed on either one of the chip and the carrier substrate; and an interconnect **12 & 24** adapted to electrically connect the electrically conductive nodes. Houston teaches lithographic alignment tolerances (col. 1, lines 49-58). In regard to claims 1, 7, 9 and 22 note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear. As to the grounds of rejection under section 103, see MPEP § 2113. Since Ho, Yao, Ferri and Houston are from the same field of endeavor (semiconductor devices), the purpose disclosed by Houston would have been recognized in the pertinent art of Ho, Yao and Ferri. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the structure of Ho by incorporating the adhesive bond of Yao, the integrateable circuit chip of Ferri and the lithographic

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alignment tolerance of Houston to provide semiconductor components capable of being closely spaced in terms of existing lithographic capabilities (col. 2, lines 1-6).

Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ho (4,254,445), Yao (6,163,068), Ferri (4,326,180) and Houston (US 6,362,117 B1) as applied to claim 1 above, and further in view of Akram (US 2001/0014488 A1).

Ho, Yao, Ferri and Houston teach all mentioned in the rejection above. However, Ho, Yao, Ferri and Houston to teach a carrier substrate, an adhesive bond, and an integrated circuit chip having essentially the same coefficient of thermal expansion (CTE). Akram teaches a carrier substrate **102**, a metal adhesive bond **112**, and an integrated circuit chip **104** having essentially the same coefficient of thermal expansion (CTE) (Figure 4, page 2, paragraph [0027]). Since Ho, Yao, Ferri, Houston and Akram are from the same field of endeavor (semiconductor devices), the purpose disclosed by Akram would have been recognized in the pertinent art of Ho, Yao, Ferri and Houston. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the structure of Ho, adhesive bond of Yao, the integrateable circuit chip of Ferri and the lithographic alignment tolerance of Houston by incorporating the CTE of Akram to increase the semiconductor die density of a semiconductor package (page 1, paragraph [0007]).

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ho (4,254,445), Yao (6,163,068), Ferri (4,326,180) and Houston (US 6,362,117 B1) as applied to claims 1 and 5-7 above, and further in view of Bayan et al. (6,372,539 B1).

Ho, Yao, Ferri and Houston teach all mentioned in the rejection above. However, Ho, Yao, Ferri and Houston fail to teach a filler to fill the gaps. Bayan et al. teach a filler material **225** adapted to fill a peripheral gap between the interior edges of each of the slots **208** and the peripheral edges of each of the integrated chips **220** when each chip is adhered within each slot (Figure 3G, col. 5, lines 29-67). Since Ho, Yao, Ferri, Houston and Bayan et al. are from the same field of endeavor (semiconductor devices), the purpose disclosed by Bayan et al. would have been recognized in the pertinent art of Ho, Yao, Ferri and Houston. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the structure of Ho, the adhesive bond of Yao, the integrateable circuit chip of Ferri and the lithographic alignment tolerance of Houston by incorporating the filler material of Bayan et al. to connect the chips to the associated areas (col. 4, lines 50-54).

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ho (4,254,445), Yao (6,163,068), Ferri (4,326,180), Houston (US 6,362,117 B1) and Bayan et al. (6,372,539 B1) as applied to claims 1, 5-7 and 10 above, and further in view of Moser et al. (4,797,780).

Ho, Yao, Ferri, Houston and Bayan et al. teach all mentioned in the rejection above. However, Ho, Yao, Ferri, Houston and Bayan et al. fail to teach a filler material

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comprising glass frit. Moser et al. teach a filler material comprising glass frit (col. 1, lines 57-63). Since Ho, Yao, Ferri, Houston, Bayan et al. and Moser et al. are from the same field of endeavor (semiconductor devices), the purpose disclosed by Moser et al. would have been recognized in the pertinent art of Ho, Yao, Ferri, Houston and Bayan et al. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the structure of Ho, the adhesive bond of Yao, the integrateable circuit chip of Ferri, the lithographic alignment tolerance of Houston and the filler material of Bayan et al. by incorporating the glass frit filler material of Moser et al. to provide impregnable filler (abstract).

Allowable Subject Matter

Claims 23 and 25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments filed 09-08-03 have been fully considered but they are not persuasive.

It is within the level of ordinary skill that the tolerances ranges between integrated circuit chip substrates are larger than the tolerance between the integrated structures on the chip substrates.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M Soward whose telephone number is 703-305-3308. The examiner can normally be reached on Monday - Thursday, 6:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 703-308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ims
December 1, 2003


PER 7/11/03
SUPERVISOR OF PATENT EXAMINERS
TECHNOLOGY CENTER